Insights into the Fracture of Si in Cu-filled Through Silicon Via (Cu-TSV) during Annealing and Post-annealing Natural Ageing

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Copper (Cu)-filled through silicon (Si) via (Cu-TSV)- a key component in the 3D integration of advanced microelectronic packages, is mainly used as the electrical conduits between the vertically stacked Si dies. Nevertheless, Cu-TSV should also retain their structural integrity over the service life of a device. However, the wide difference in the coefficient of thermal expansion between Cu and Si generates the large thermal stresses when Cu-TSV gets subjected to the different thermal excursions, e.g., during fabrication of microelectronic devices or due to on-off cycles of the device during their regular operation. These thermal stresses can lead to serious reliability concerns in the Cu-TSV systems, such as fracture of Si wafer, creep in Cu, Cu-Si interface delamination, etc. In this work, fracture of Si wafer comprised of Cu-TSV was observed due to the annealing in the temperature range of 250–550 °C and subsequent natural ageing. The failure of the diffusion barrier layer placed between Cu and Si was observed due to the generated thermal stresses followed by the nucleation of micro-cracks in Si in the vicinity of the Cu interconnect. Subsequently, microcrack propagation at a constant velocity was observed during post-annealing room temperature ageing, thereby substantiating slow crack growth in Si. Microstructure examinations in addition to the stress measurement using Raman spectroscopy and FEA revealed that volumetric strain applied by Cu-Si compound leads to the microcrack nucleation in Si, whereas oxidation of Si at the crack tip was found as the driving force for the delayed fracture in Si.